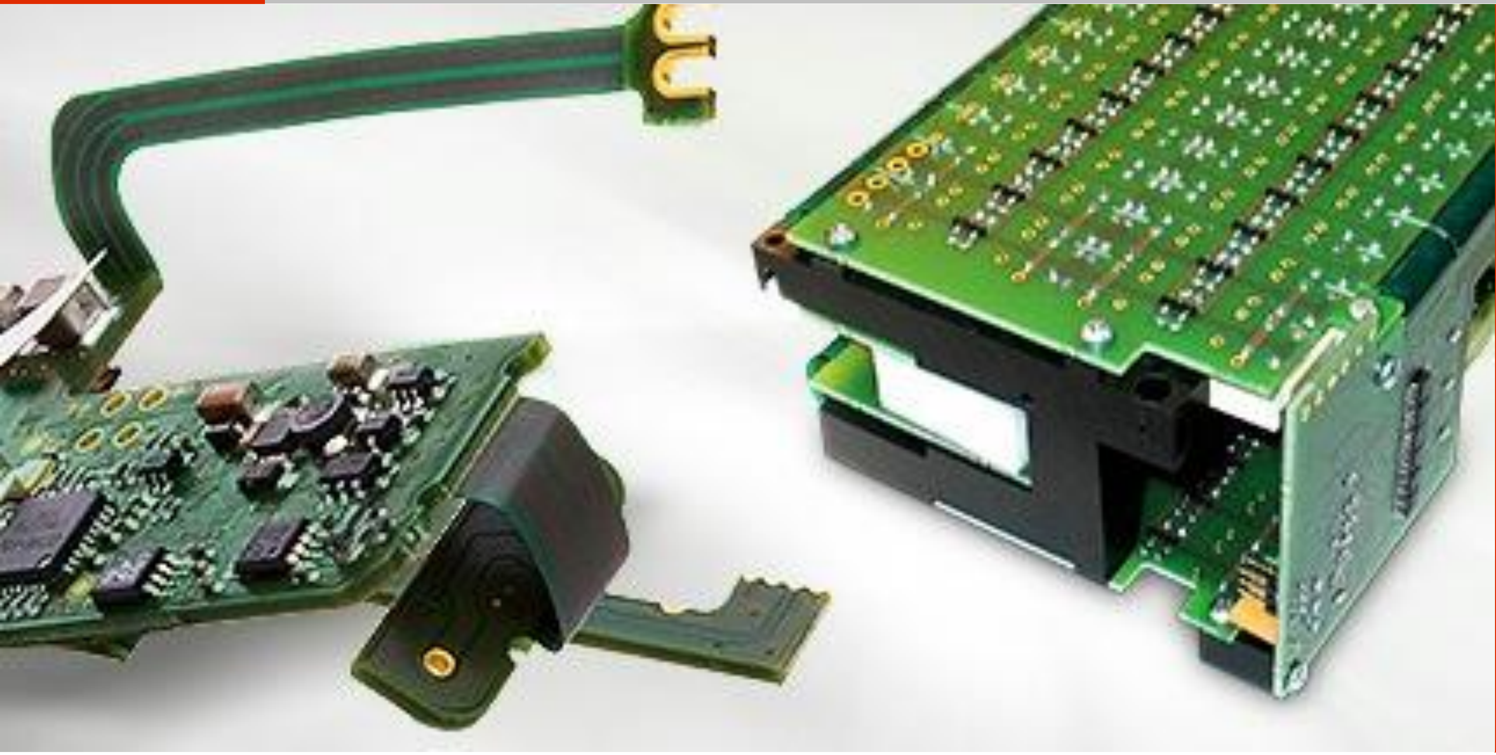
Flex-rigid in combination with USB3

Würth Elektronik Circuit Board Technology



Webinar October 10, 2017

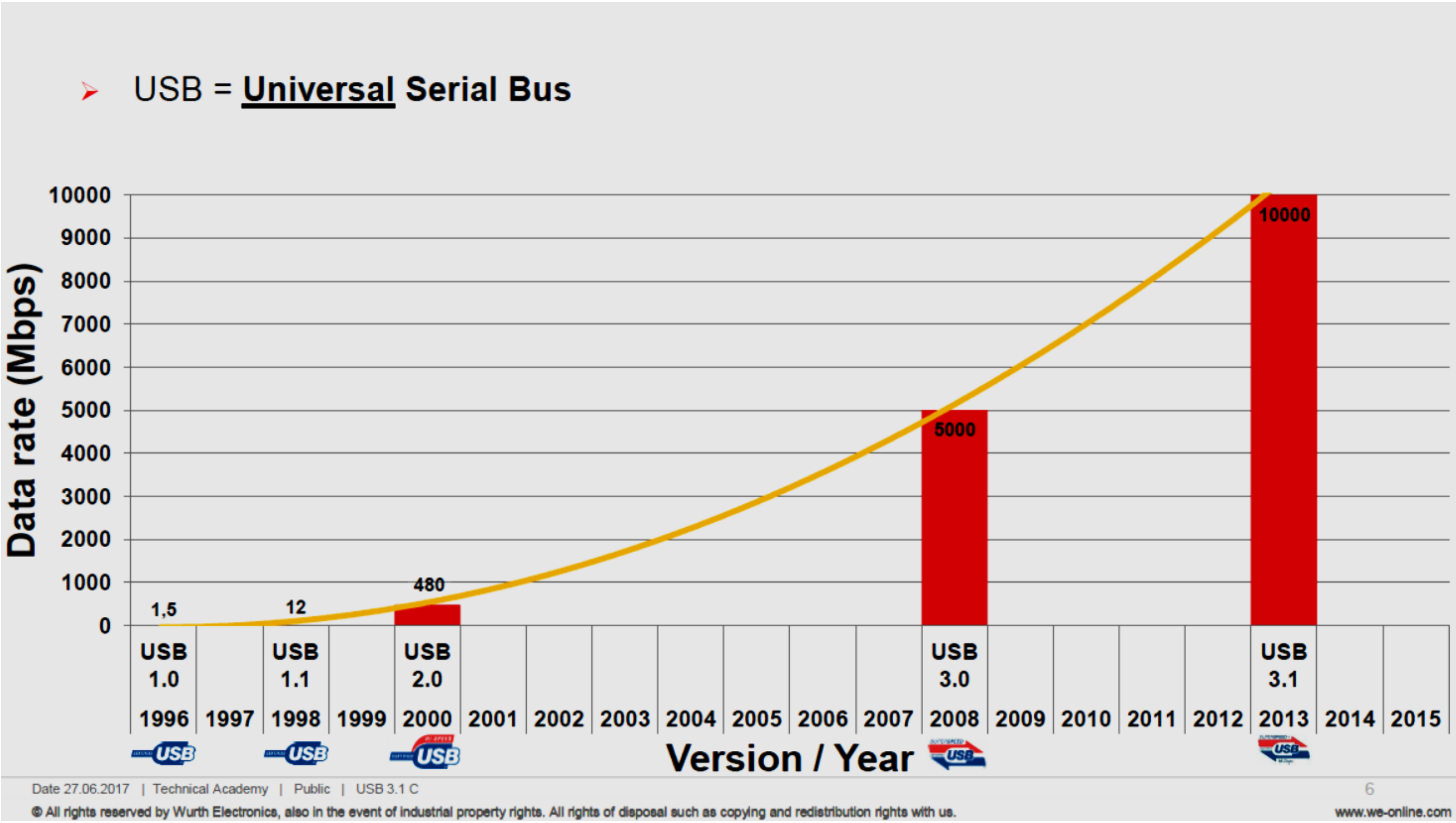
Speaker: Andreas Schilpp

Agenda

- Interfaces
- Signal integrity with Flex-rigid
- Design Chain – Concept Flow
- Applications
- Summary, Q&A

Interfaces

- **Development USB = Universal Serial Bus**
  - **Data rate**



source: WE USB3.X Kongress

Interfaces

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- **Development USB = Universal Serial Bus**
  - **Benchmark**

➢ Based on Microsoft tests: (showed at WinHEC 2008 on Nov 6)

Transfer of a 25GB Blu-ray movie:
USB 1.1: 9.3 hours
USB 2.0: 13.9 minutes
USB 3.0: 70 seconds

≈ x 40

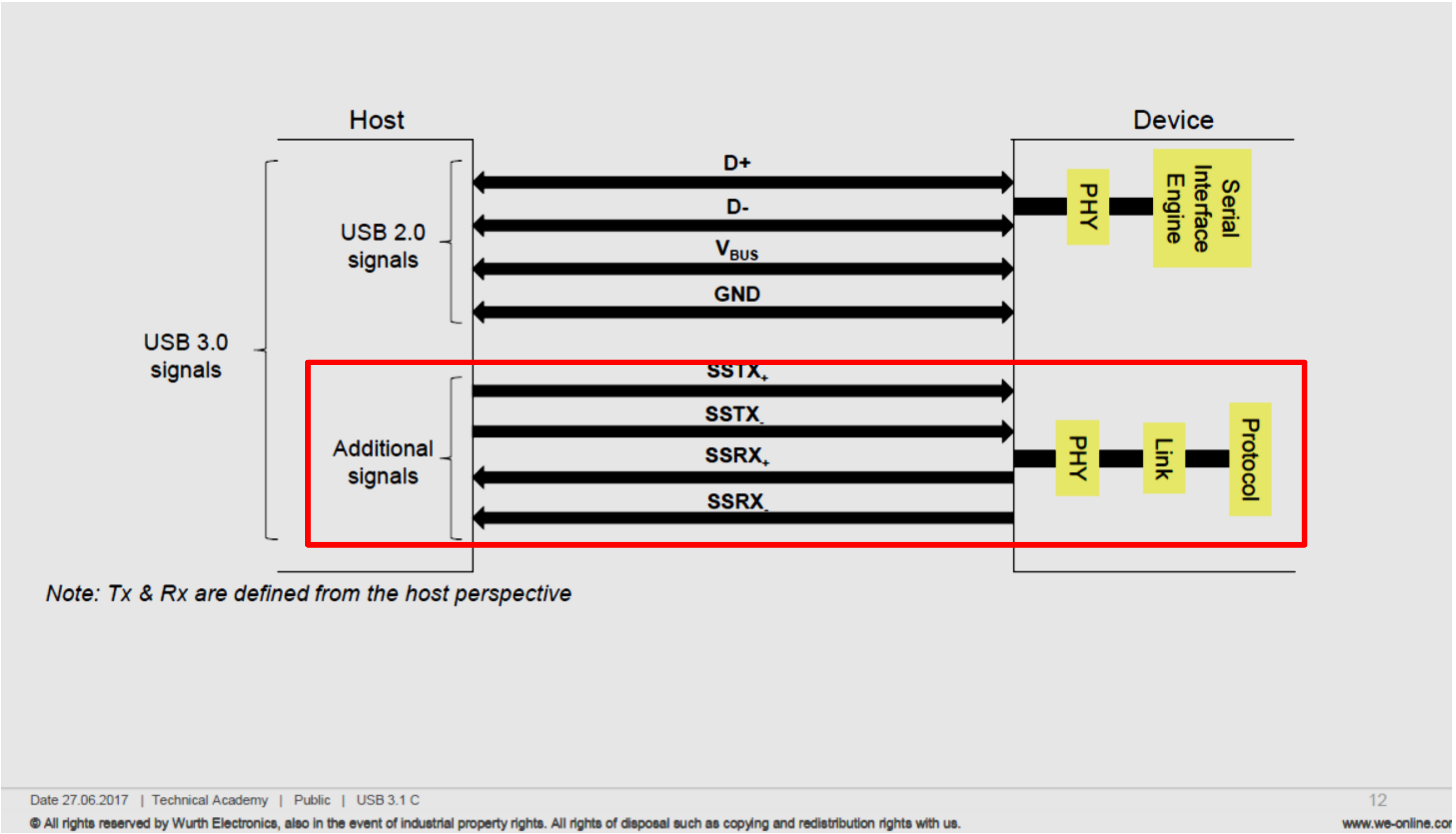
≈ x 12

USB version	Data rate
USB 1.0	1,5 Mbps
USB 1.1	12 Mbps
USB 2.0	480 Mbps
USB 3.0	5 Gbps
USB3.1Gen.2	**10 Gbps**

source: WE USB3.X Kongress

Interfaces

- **additional wires: 2x diff. pairs**



source: WE USB3.X Kongress

Interfaces

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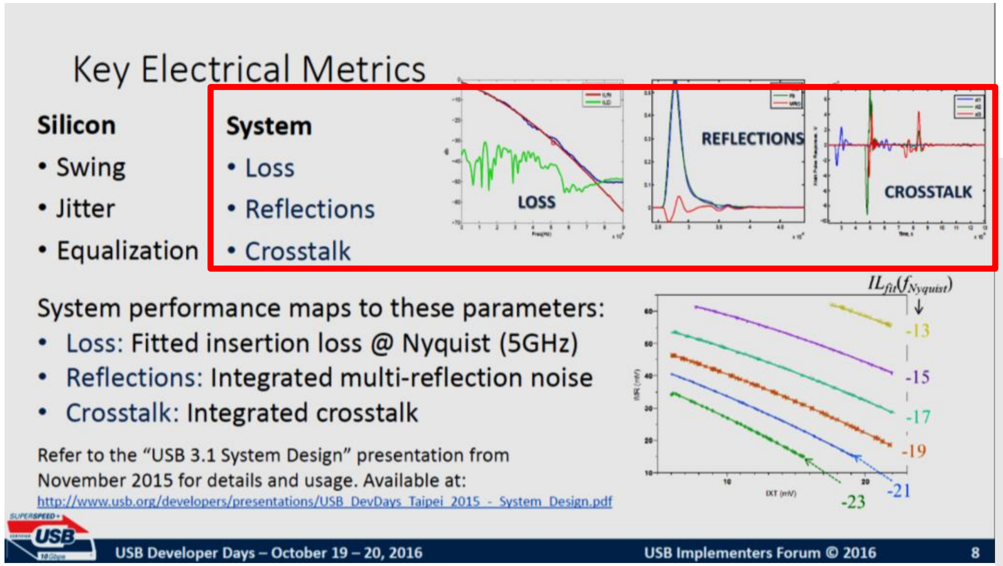
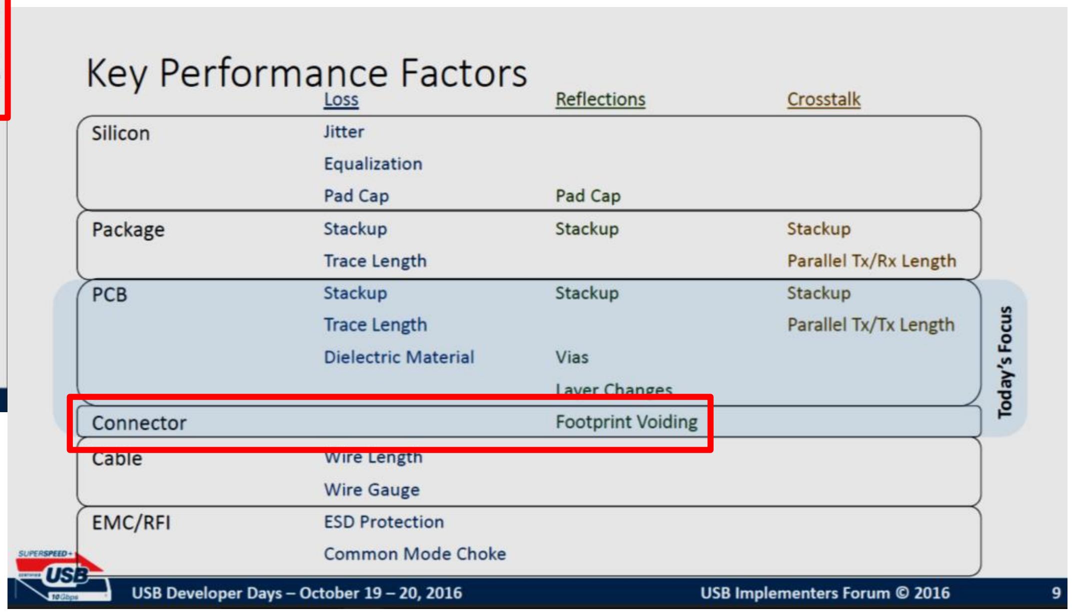
- **USB (Universal Serial Bus) Zdiff 90 ohms**
- **LVDS (Low-Voltage-Differential Signaling) Zdiff 100 ohms**

- **<u>Challenge for the PCB:</u>**



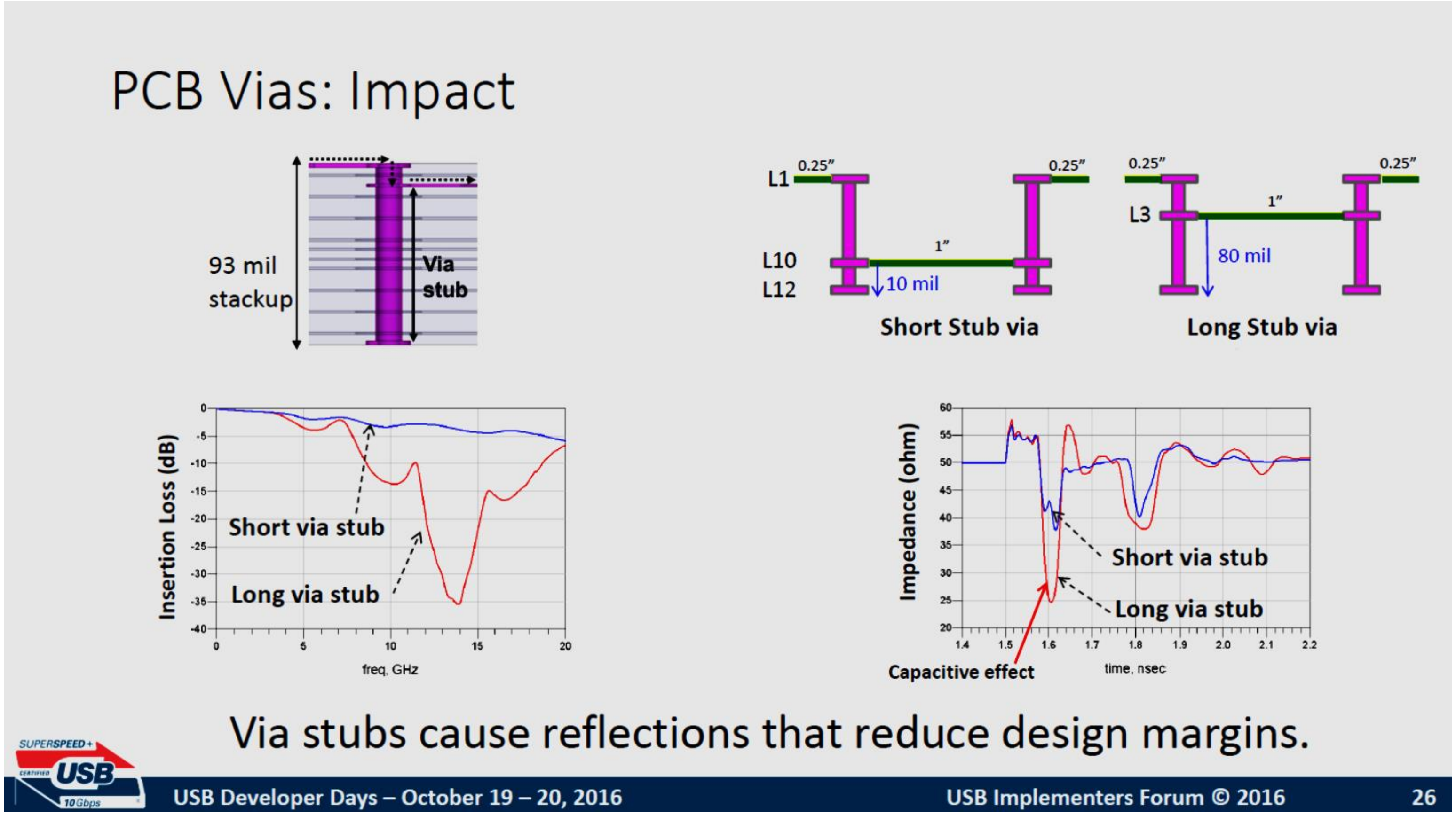


source: USB Implementers Forum 2016

Interfaces

Approach: Microvias and Flex-rigid

- **Avoiding of THV when ever possible**



source: USB Implementers Forum 2016

Interfaces

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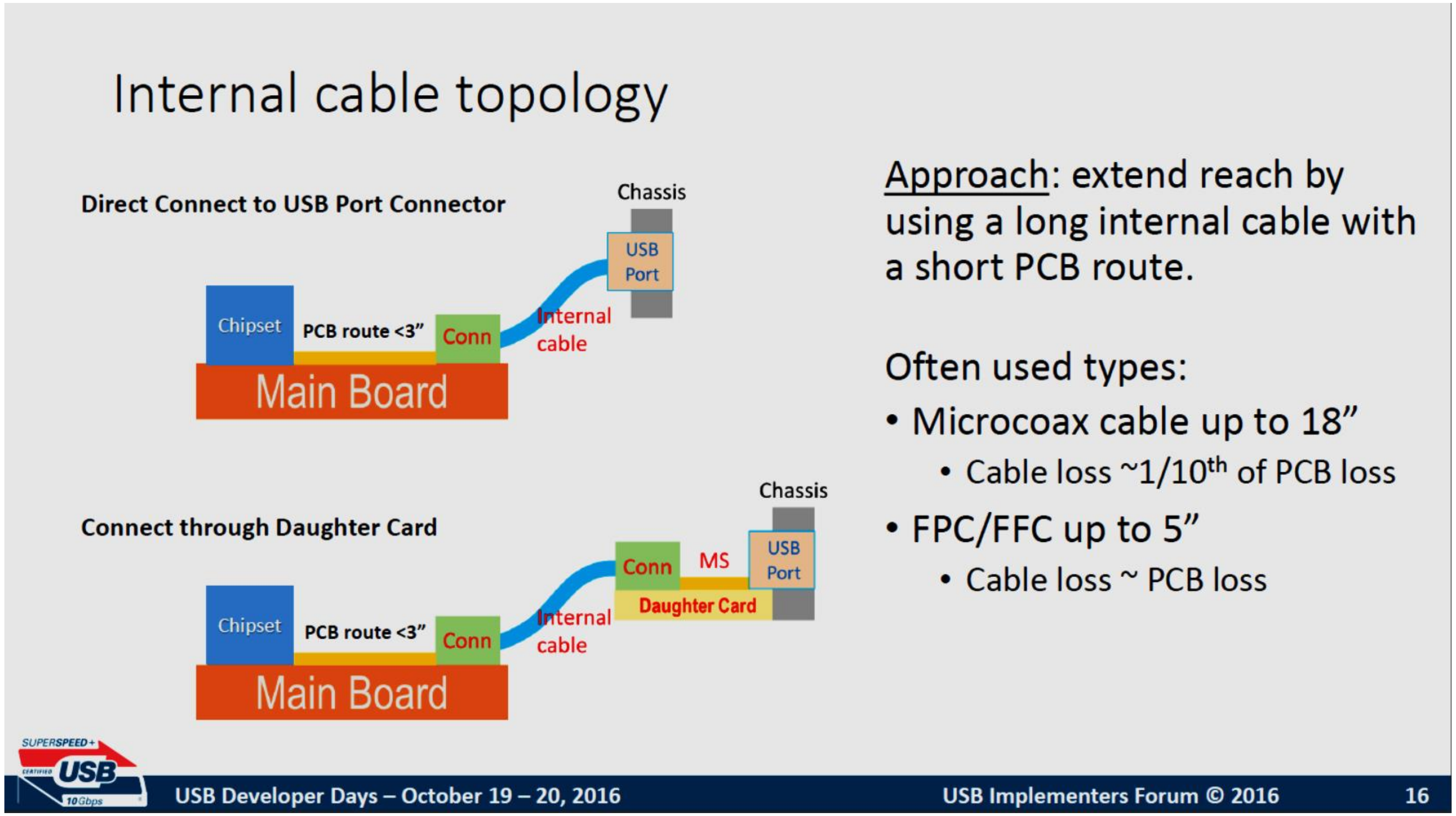
Approach: Flex-rigid Technology

- **low-loss Material Polyimide**
- **Elimination of weak point „connector“**



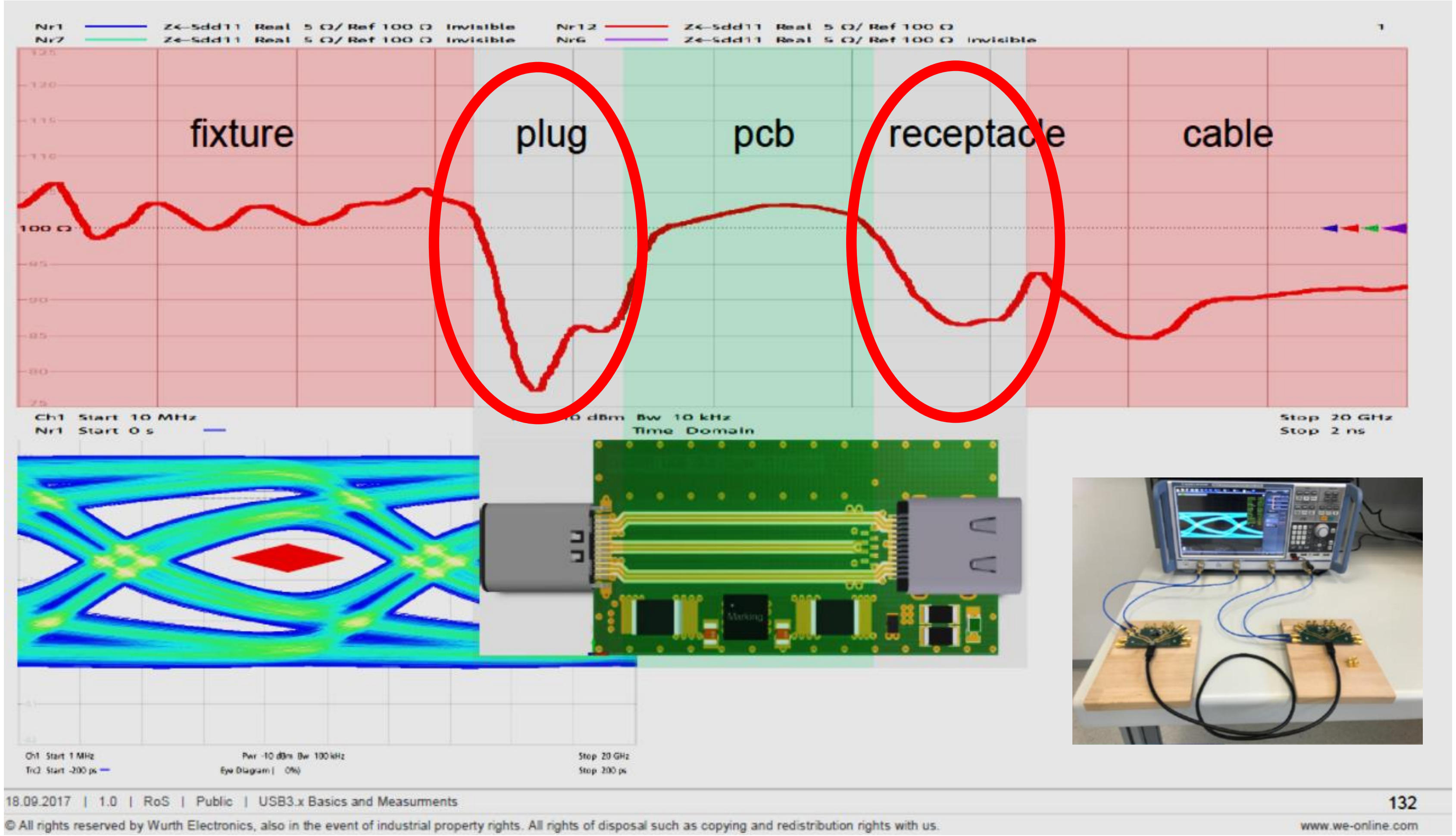
source: USB Implementers Forum 2016

Interfaces

source: WE USB3.X Kongress

Approach: Flex-rigid Technology

- Elimination of weak point „connector



Agenda

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- Signal integrity with Flex-rigid
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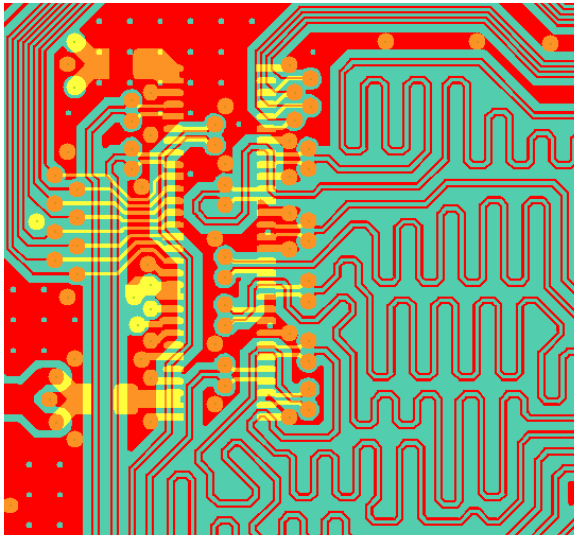
Signal integrity and the PCB

Major topics:

- **Impedance power matching**
- **Signal time (Timing) / bus timing**
- **Reflections**

Example from USB3-design:



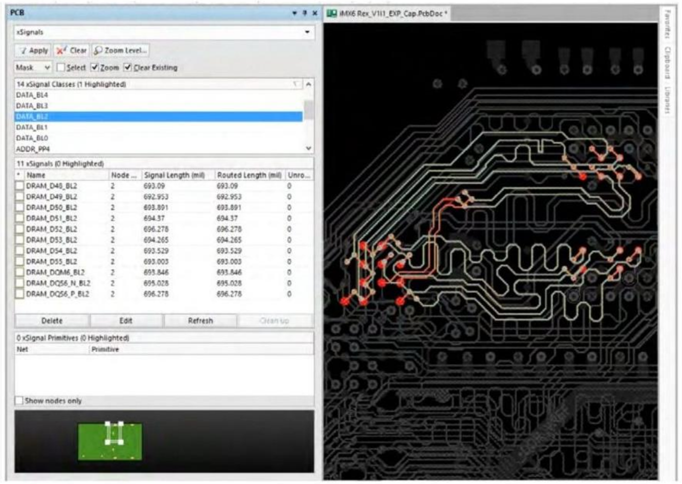


Figure 2: Automatically generated xSignal Class of all Byte Lane 2 specific Data xSignals

source: Altium

<u>TIPP:</u>
More informations about Signal Integrity with Flex-rigid technology: Webinar Archive

[here]

Specialties with flex-rigid: Flexible material Polyimide

- **PI in general performs good for high frequencies because**
  - **small losses due to small value of tanδ (loss tangent)**
  - **small losses due to very low Treatment of copper**
- **in general „need of action“ because of**
  - **small value of dielectric constant**
  - **small thickness of dielectic material, typ. 50µm**

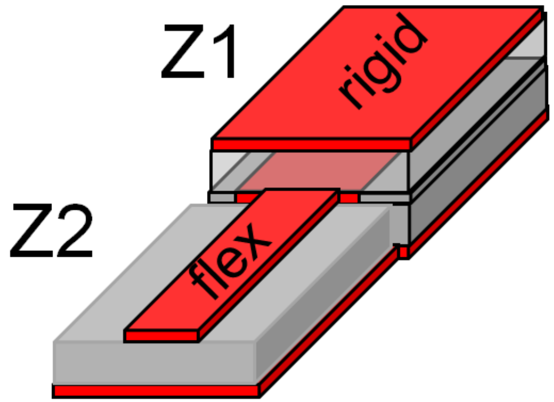


Figure 6. Dielectric Constant vs. Frequency

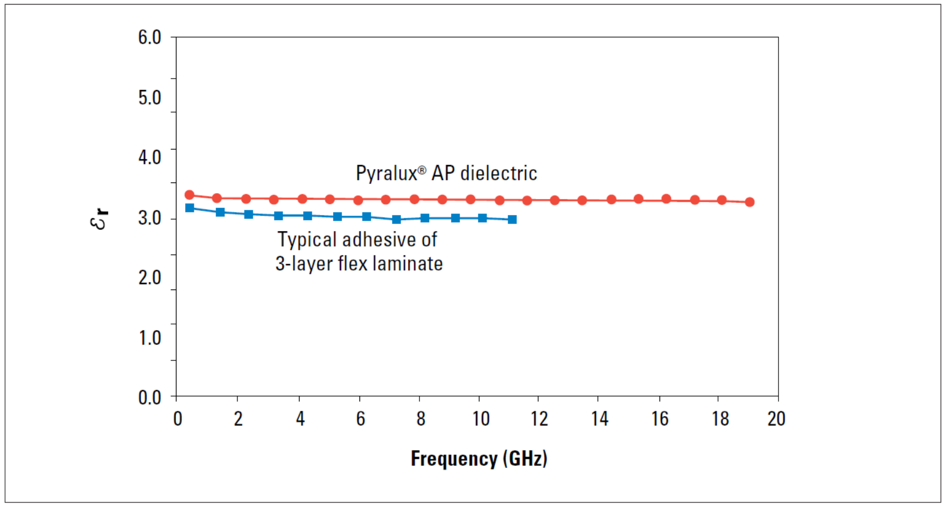
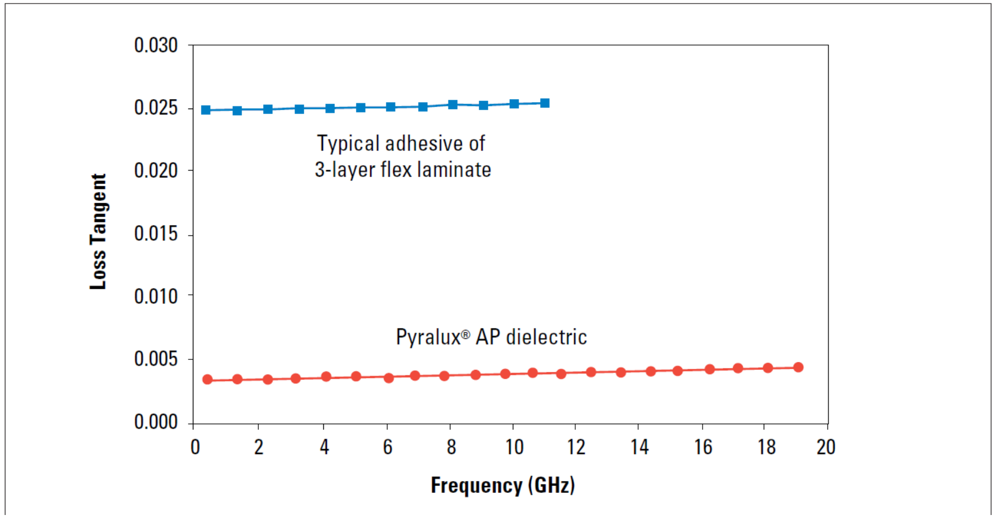
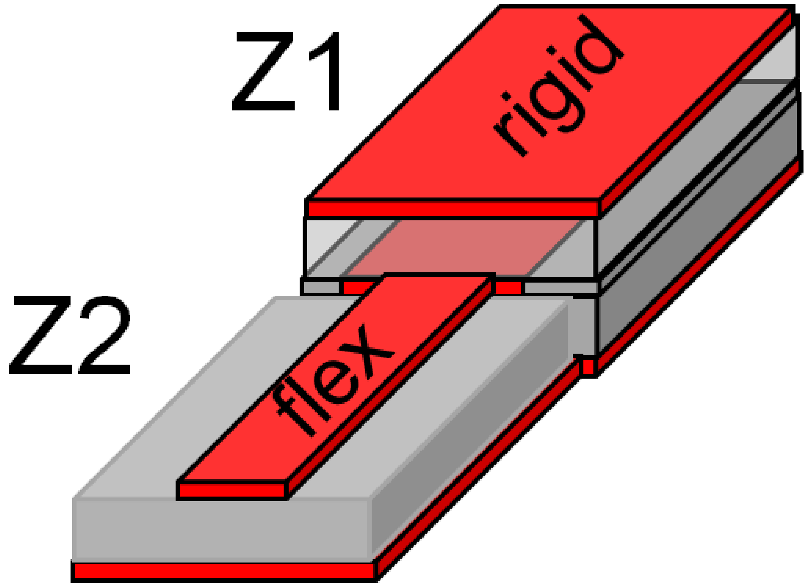


Figure 7. Loss Tangent vs. Frequency



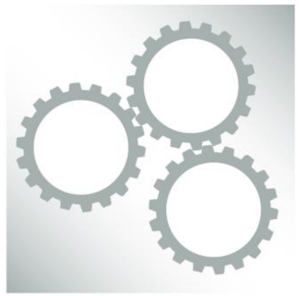
Specialties with flex-rigid



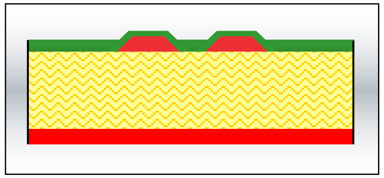
$Z_{flex} = Z_{rigid}$

Solution:

- **Define target impedance value**
- **Choose impedance model**
- **Choose H of flexible layer (thickness PI)**
  - (! 75µm / 100µm PI are cost drivers!)
  - ? Are there mechanical requirements? (i.e. bending radii, dynamical bendings?)
- **Simulation: fit line width consider W_{min} with PCB producer**
- **„Hatch“ - Option for reference layer**

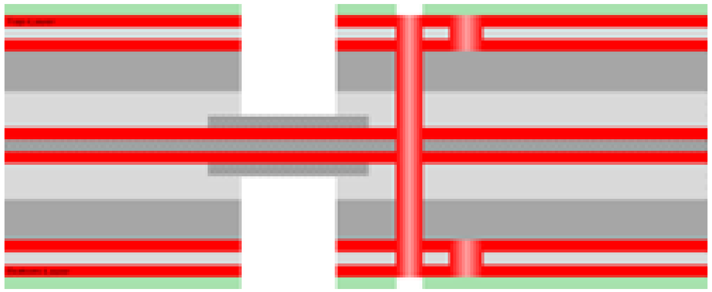


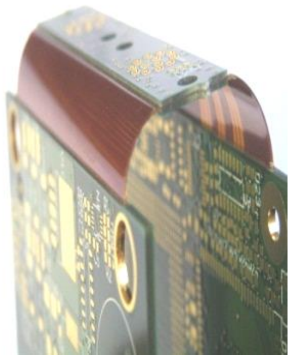
Layer Configuration: 2 layers in Flex- / Bending Area



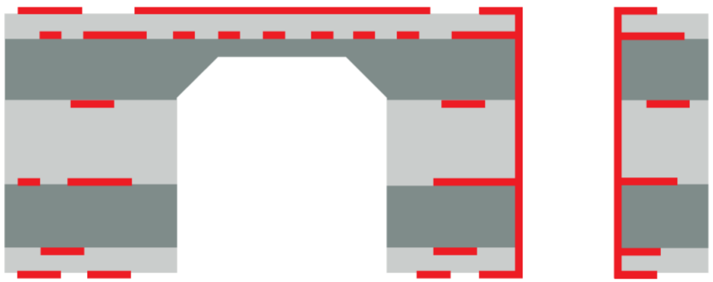
Edge Coupled Coated Microstrip – with 1 Reference layer

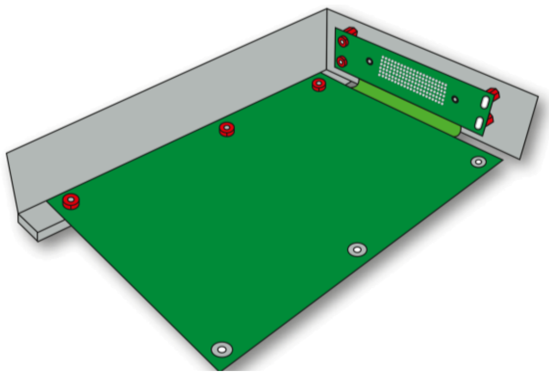
- **Flex-rigid xRi–2F–xRi**



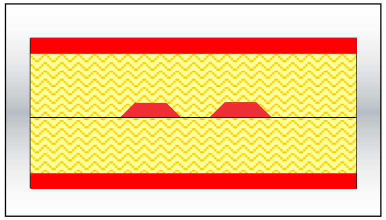


- **FR4 Semiflex 2Ri–xRi**



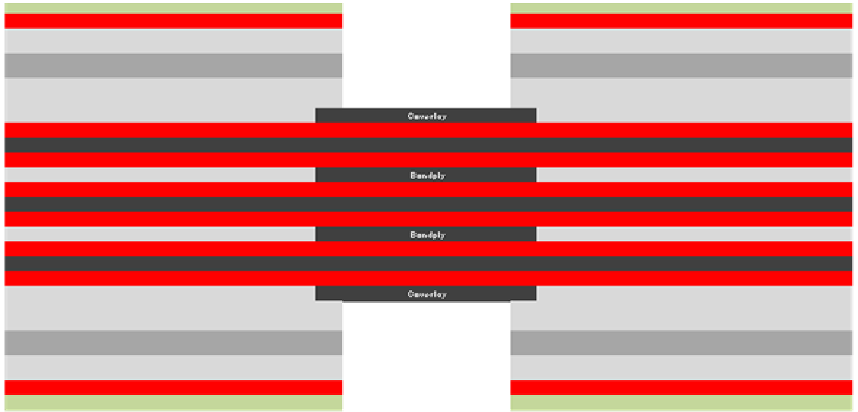


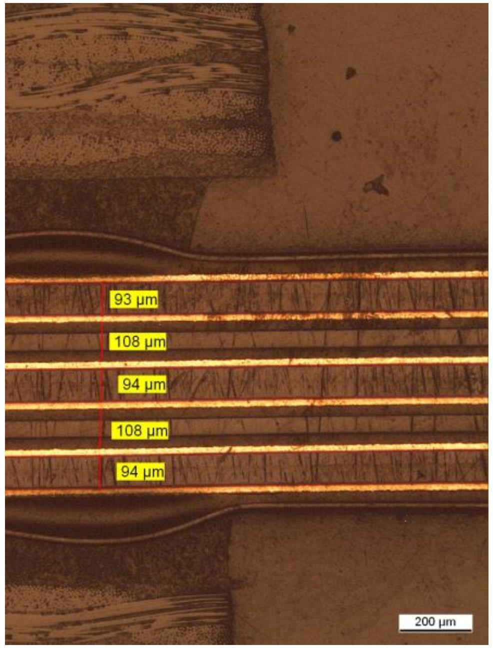
Layer Configuration: > 2 layers in Flex area



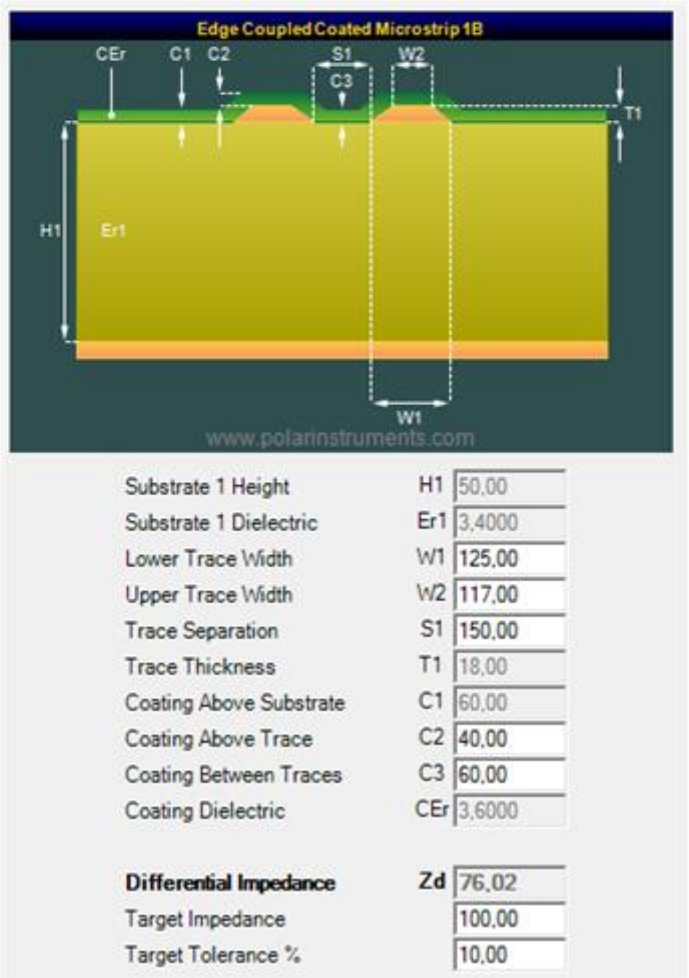
Stripline – with 2 Reference layers

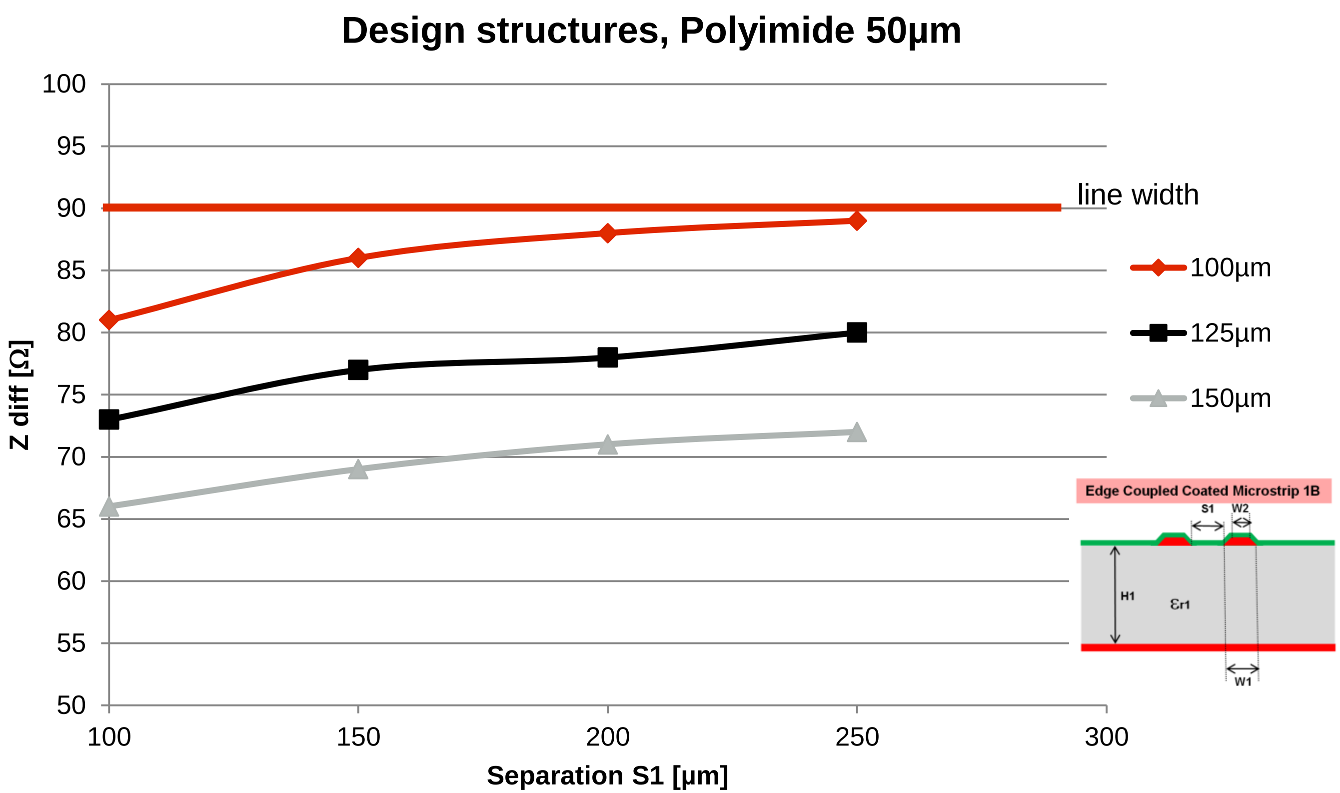
- **Flex-rigid > xRi–2F–xRi, z.B. 1Ri–6F–1Ri**





Effect of line / space Parameters





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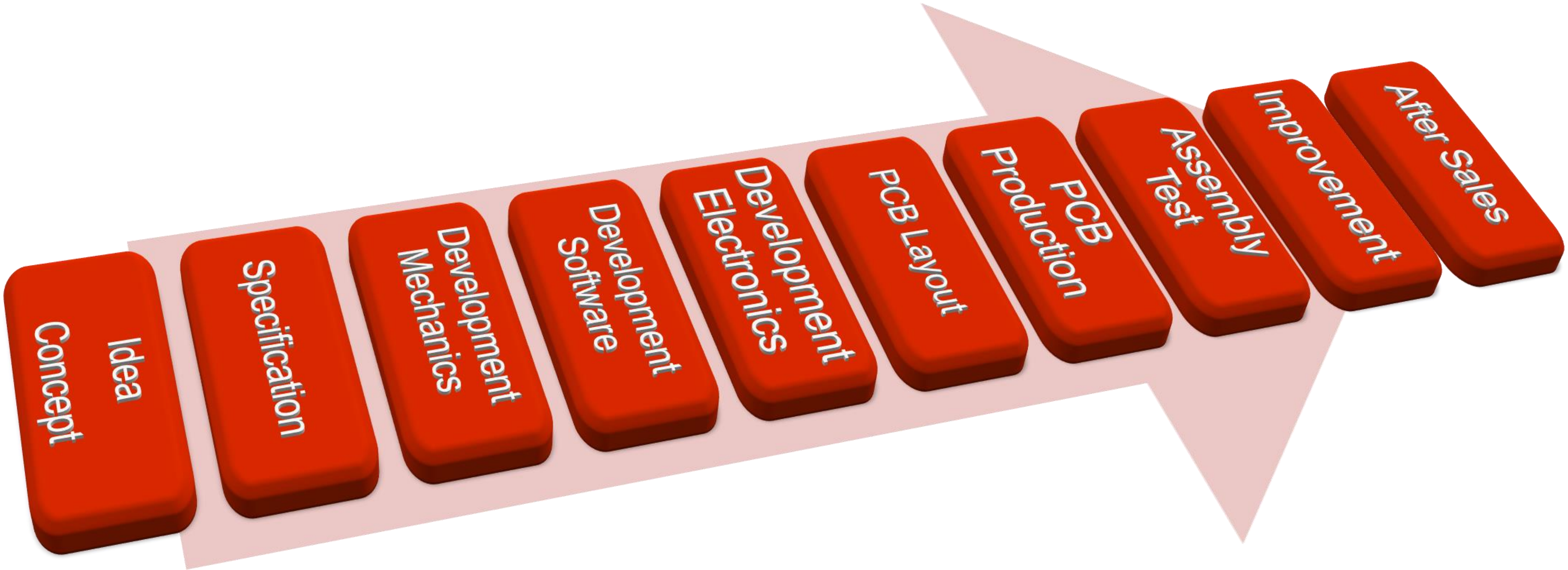
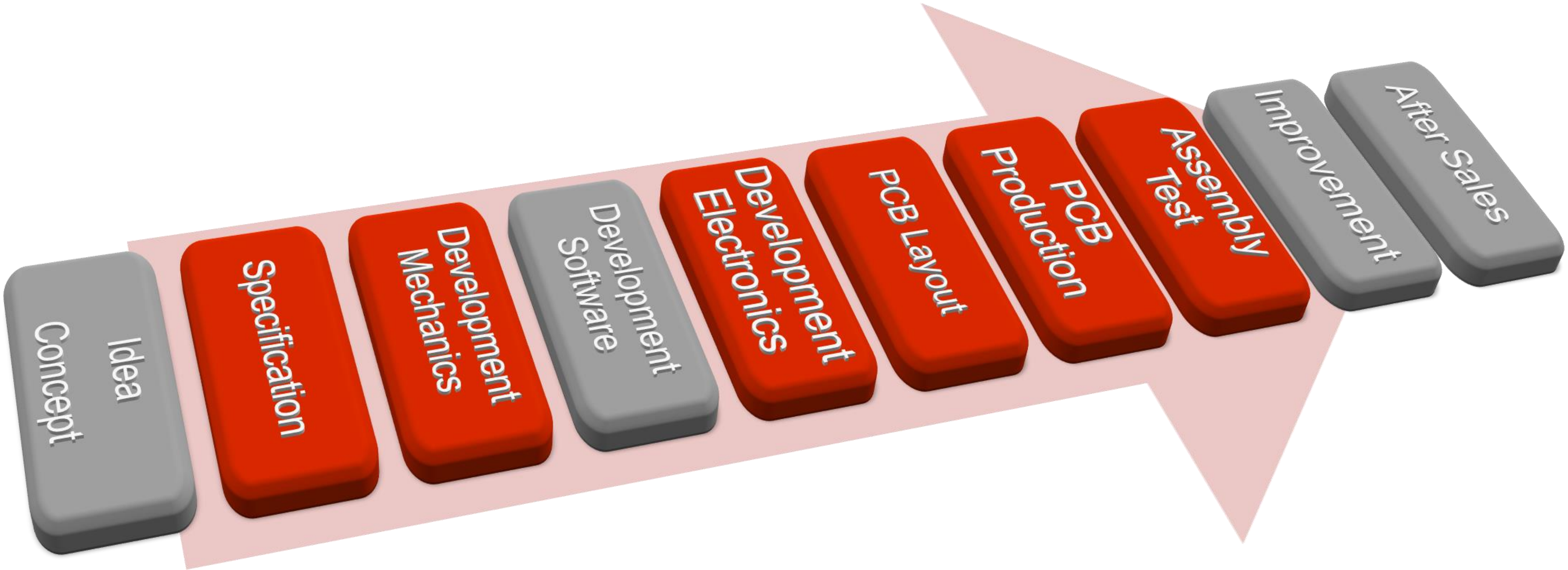
Design Chain of the development of electronic equipment



More information about Design Chain you could find *[here]()*

Design Chain for Flex-rigid and high data rates



important input for the following approach

Flow „Flex-rigid with Impedance Specification“

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components
- Stack-up (Standard)
- Via Technology

mechanical Design
- Check Area consumption (Design, Testcoupon?)
- Cost optimization

SI Specification
- Adaption of Stack-up
- Impedance calculation, Impedance Documentation
- Quote Flex-rigid pcb

Elektronical Design
- Order with Impedance Documentation, Production PCBs
- with / without Testcoupon / Impedance test (Serie?)

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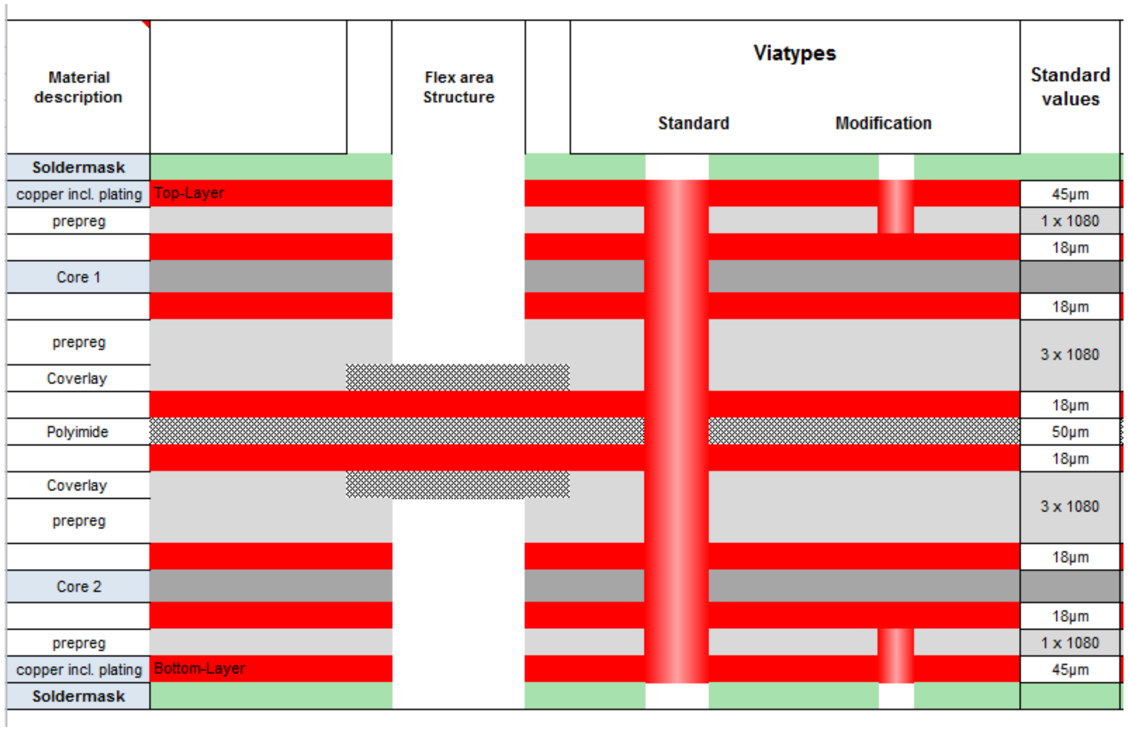
Standard Stack-up Plans for Flex-rigid Technology

- Base material Standard xRi-2F-xRi
  - Rigid: FR4 Tg ≥150°C, halogen free, filled
  - Flex: Polyimide Tg > 200°C – typical 50µm thick
  - Soldermask, Polyimide Coverlay „Bikini“
  - Copper thickness inner layers 18µm

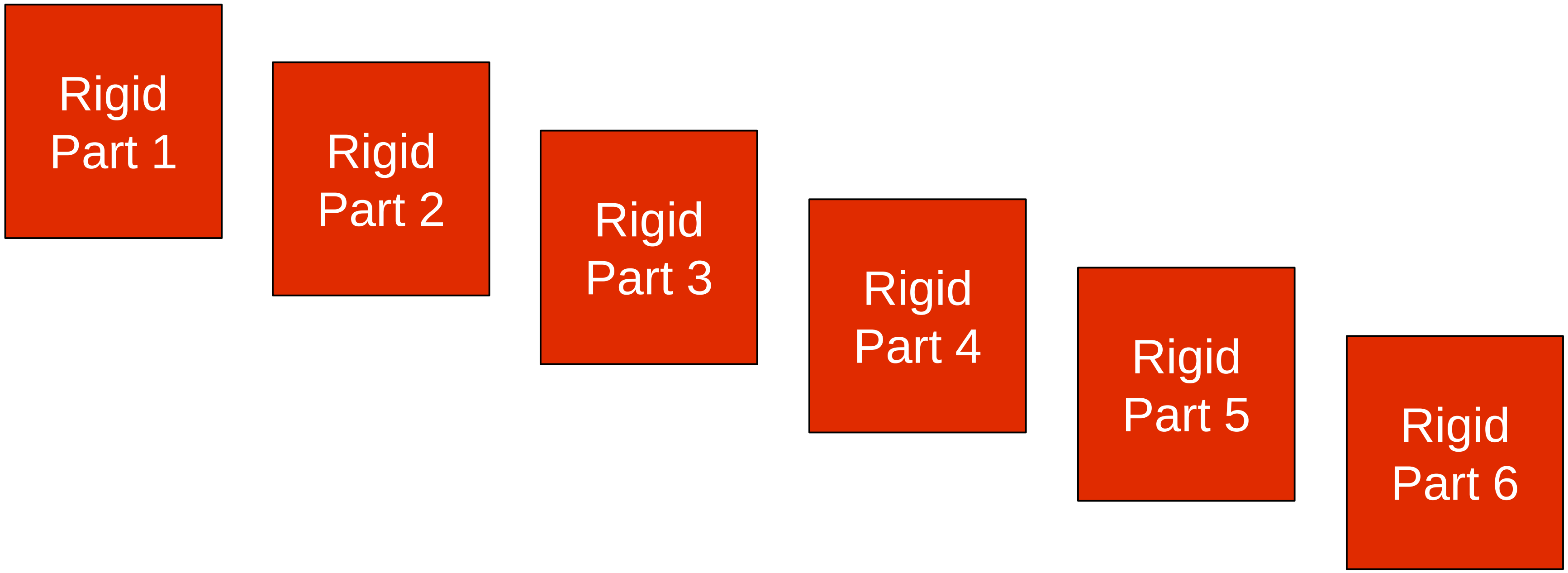


Hint:

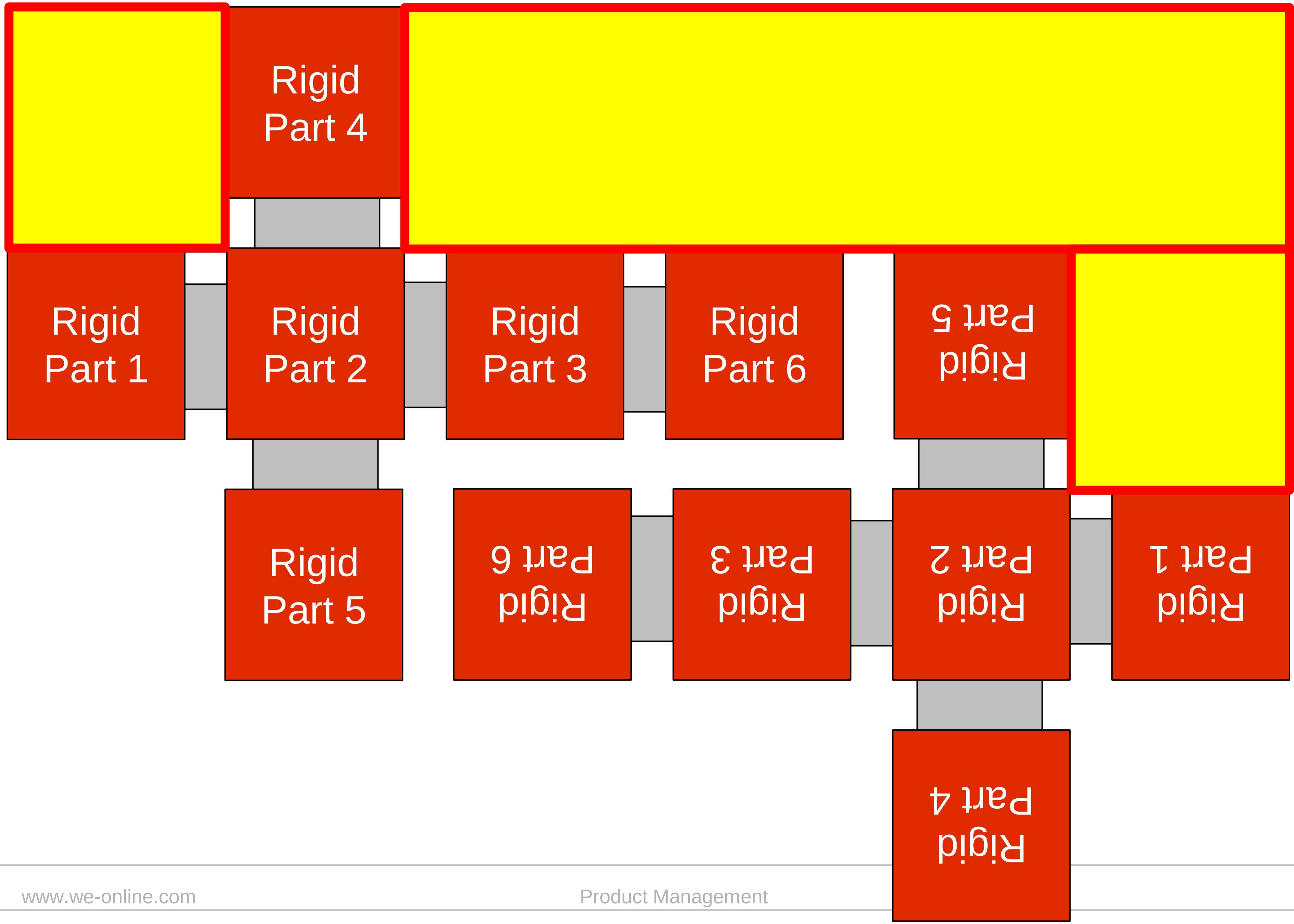
For enquiries please use our Team address:

flex@we-online.com

Mechanical Design
Area consumption of different Approaches

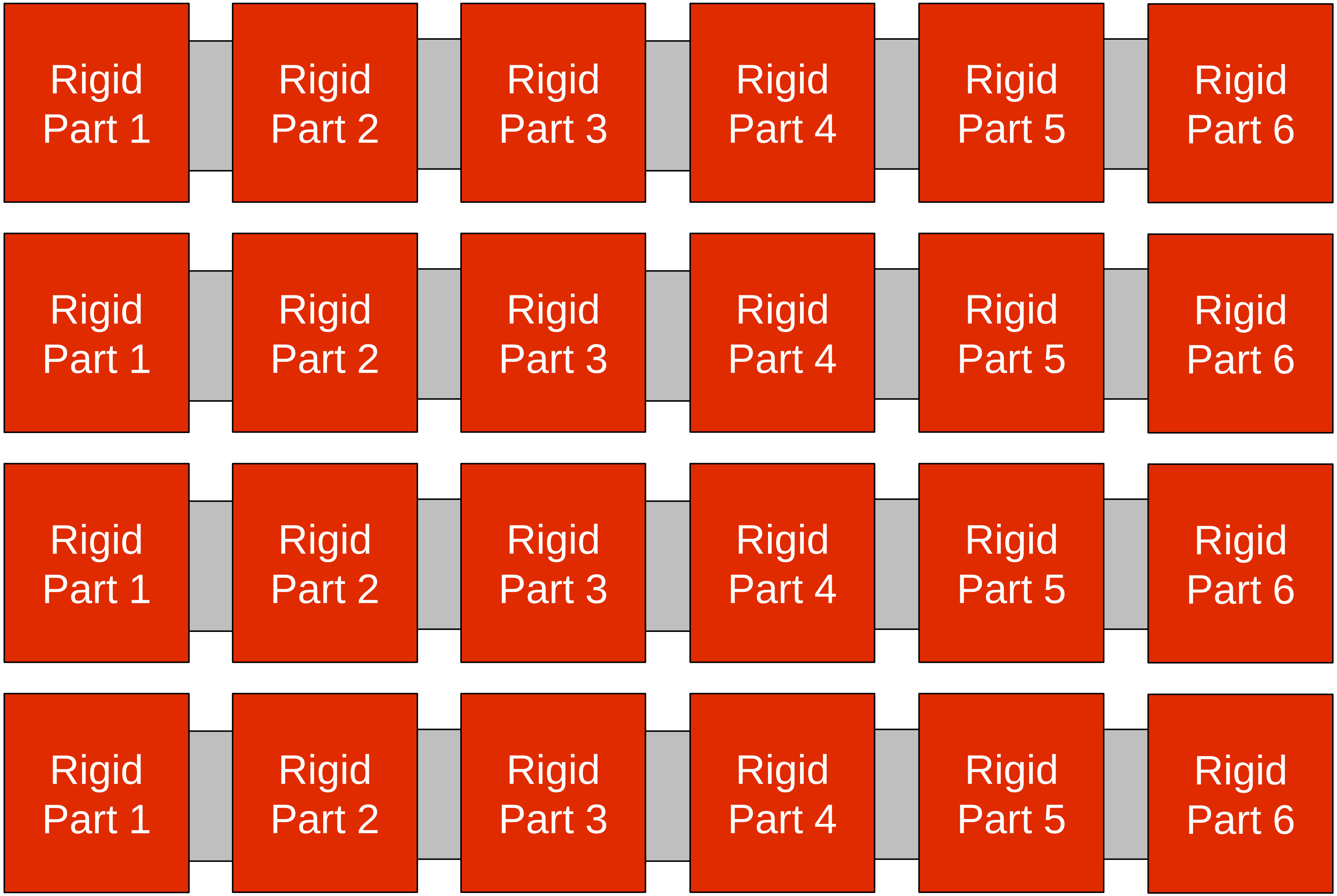


Mechanical Design
Area consumption „Cross“

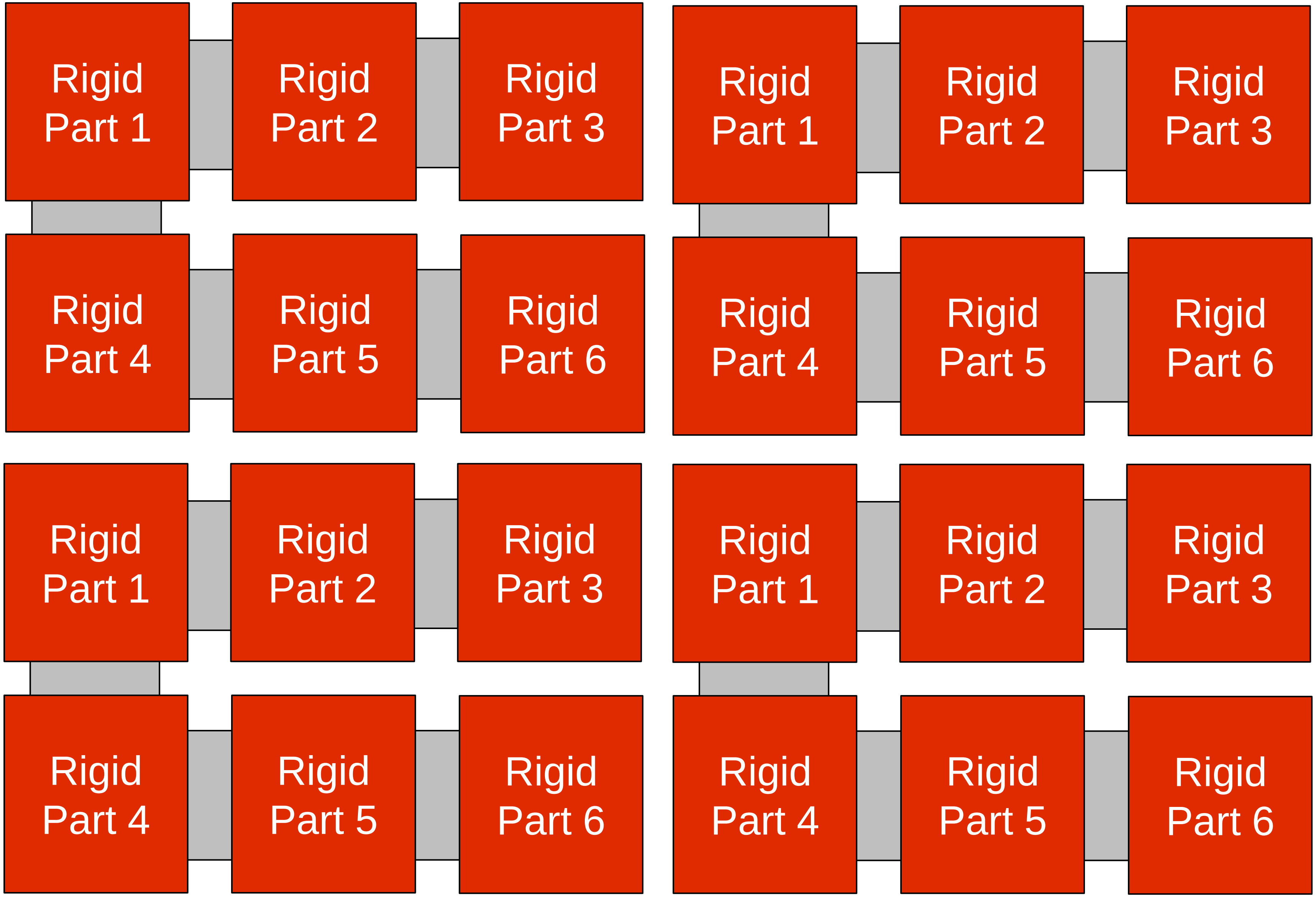


Mechanical Design
Area consumption „L-Form“

Mechanical Design
Area consumption „Line“

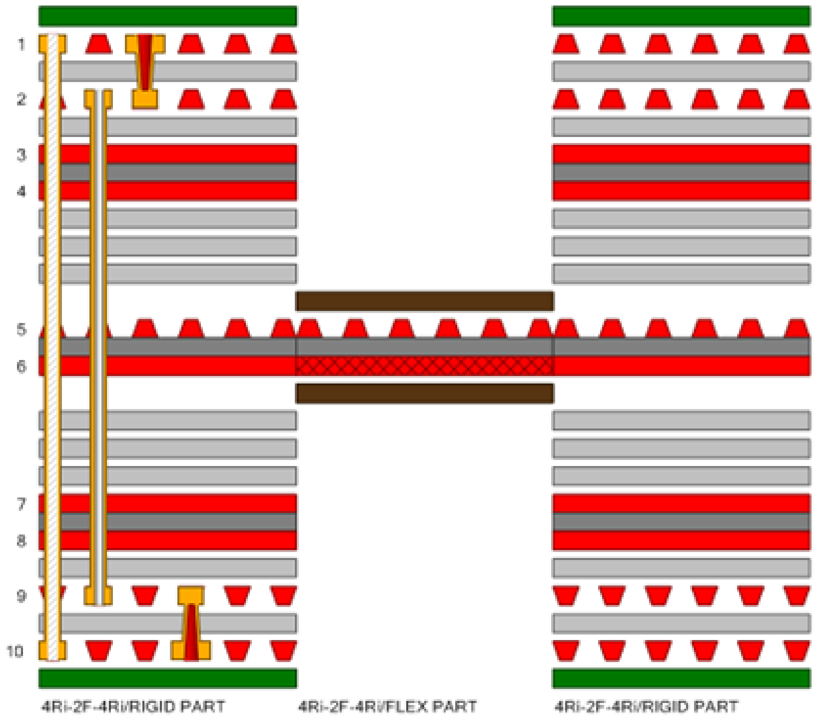


Mechanical Design
Area consumption „Matrix“

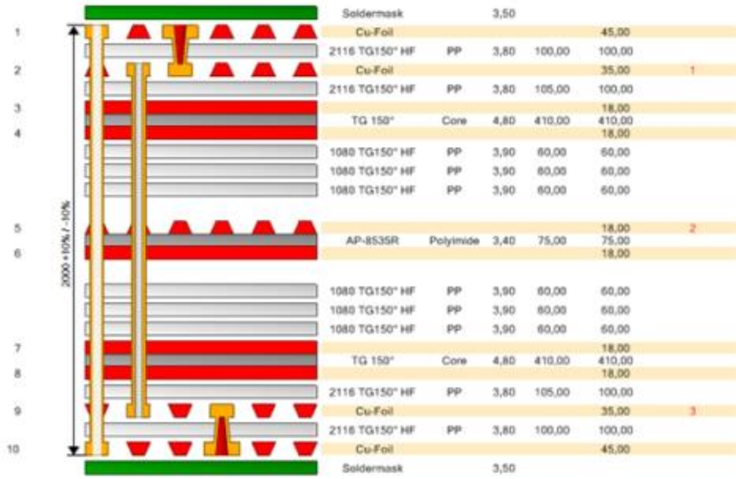


Adjusting Stack-up

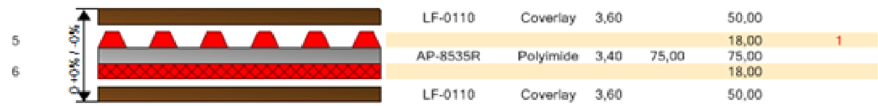
Master View:



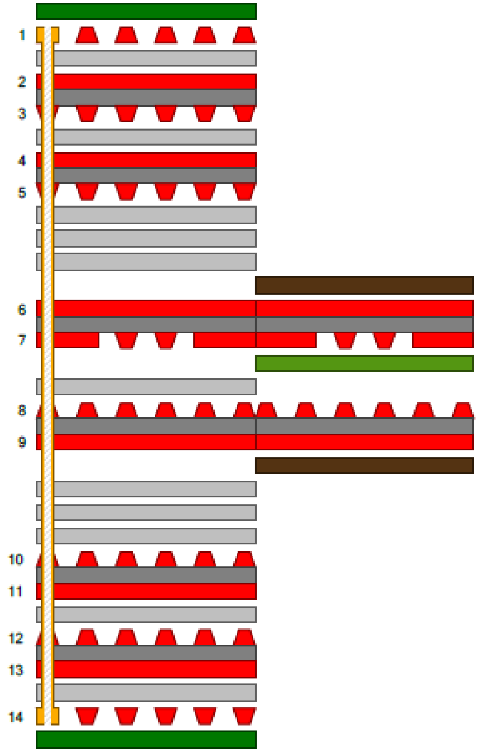
View Rigid Area:



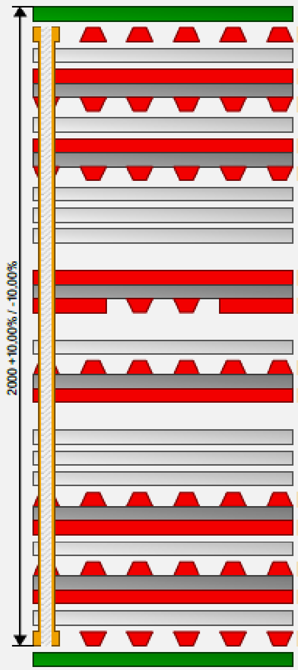
View flexible Area:



Calculation and Documentation 5Ri-4F-5Ri



5Ri-4F-5Ri_2,0_18_100µmPi... 5Ri-4F-5Ri_2,0_18_100µmPi...



Layer	Stack up	Description	Type	εr	Processed Thickness	Mask Thickness	Impedance ID
		Soldermask		3,50		40,00	
1		Cu-Foil			35,00		1, 2, 3
		2116 TG150° HF	PP	3,80	100,00		
2					18,00		
		TG 150°	Core	3,90	150,00		
3					18,00		4, 5, 6, 7
		2116 TG150° HF	PP	3,80	100,00		
4					18,00		
		TG 150°	Core	3,70	125,00		
5					18,00		8, 9, 10, 11
		1080 TG150° HF	PP	3,90	60,00		
		1080 TG150° HF	PP	3,90	60,00		
		1080 TG150° HF	PP	3,90	60,00		
6					18,00		
		AP-8545R	Polyimide	3,40	100,00		
7					18,00		12, 13, 14, 15
		2116 TG150° HF	PP	3,80	100,00		
8					18,00		16, 17
		AP-8545R	Polyimide	3,40	100,00		
9					18,00		
		1080 TG150° HF	PP	3,90	60,00		
		1080 TG150° HF	PP	3,90	60,00		
		1080 TG150° HF	PP	3,90	60,00		
10					18,00		
		TG 150°	Core	3,70	125,00		
11					18,00		
		2116 TG150° HF	PP	3,80	100,00		
12					18,00		
		TG 150°	Core	3,90	150,00		
13					18,00		
		2116 TG150° HF	PP	3,80	100,00		
14		Cu-Foil			35,00		
		Soldermask		3,50		40,00	

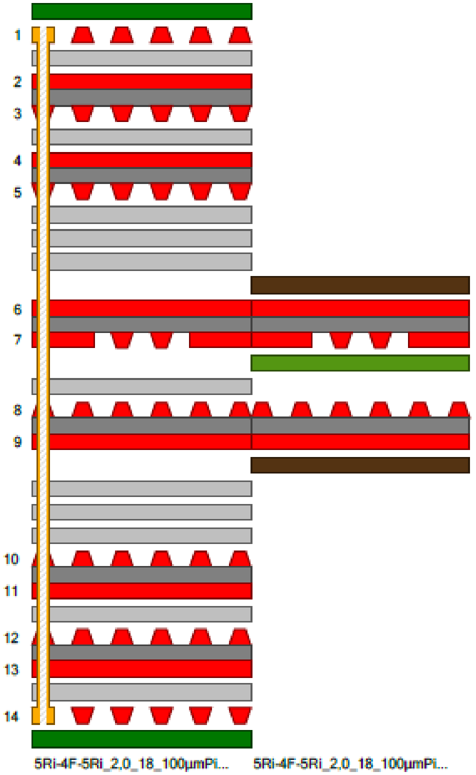
Copper Thickness = 286,000 | Dielectric Thickness = 1610,000 | Solder Mask Thickness = 80,000 | Stack Up Thickness = 1896,000 | Stack Up Thickness with Soldermask = 1976,000 |

Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Target Impedance	Calculated Impedance	Tol (+/- %)	Lower Trace Width (W1)	Trace Separation (S1)

StackName: 5Ri-4F-5Ri_2,0_18_100µmPi/RIGID	Version:	Revision:	Modification:	Date of Revision:	Editor	Page 2/5
Date: 06.08.14	Associated Documents:					
Author: W.Öchslen						
Department:						
Site:						

Software SI9000 + Speedstack
www.polarinstruments.com

Calculation and Documentation 5Ri-4F-5Ri



Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Target Impedance	Calculated Impedance	Tol (+/- %)	Lower Trace Width (W1)	Trace Separation (S1)
1		Edge Coupled Coated Microstrip 1B	1	2	0	90,00	90,60	10,00	140,00	125,00
2		Edge Coupled Coated Microstrip 1B	1	2	0	100,00	100,06	10,00	120,00	150,00
3		Coated Microstrip 1B	1	2	0	50,00	50,00	10,00	170,00	0,00
4		Edge Coupled Offset Stripline 1B1A	3	2	4	100,00	99,41	10,00	100,00	250,00
5		Offset Stripline 1B1A	3	2	4	50,00	49,67	10,00	105,00	0,00
6		Offset Stripline 1B1A	3	2	4	40,00	40,04	10,00	160,00	0,00
7		Edge Coupled Offset Stripline 1B1A	3							
8		Offset Stripline 1B1A	5							
9		Edge Coupled Offset Stripline 1B1A	5							
10		Offset Stripline 1B1A	5							
11		Edge Coupled Offset Stripline 1B1A	5							
12		Offset Stripline 1B2A	7							

StackName: 5Ri-4F-5Ri_2,0_18_100µmPi/RIGID	Version:
Date: 06.08.14	Associat
Author: W.Öchslen	
Department:	
Site:	

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Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Target Impedance	Calculated Impedance	Tol (+/- %)	Lower Trace Width (W1)	Trace Separation (S1)
13		Offset Stripline 1B2A	7	6	9	40,00	39,57	10,00	200,00	0,00
14		Edge Coupled Offset Stripline 1B2A	7	6	9	80,00	79,45	10,00	170,00	150,00
15		Edge Coupled Offset Stripline 1B2A	7	6	9	100,00	100,82	10,00	100,00	150,00
16		Offset Stripline 1B1A	8	7	9	40,00	40,72	10,00	135,00	0,00
17		Edge Coupled Offset Stripline 1B1A	8	7	9	80,00	79,48	10,00	130,00	150,00

Drill Image	1st Layer	2nd Layer	Column Position	Drill Type
	1	14	1	Mechanical PTH

Notes

StackName: 5Ri-4F-5Ri_2,0_18_100µmPi/RIGID	Version:	Revision:	Modification:	Date of Revision:	Editor	Page 4/5
Date: 06.08.14	Associated Documents:					
Author: W.Öchslen						
Department:						
Site:						

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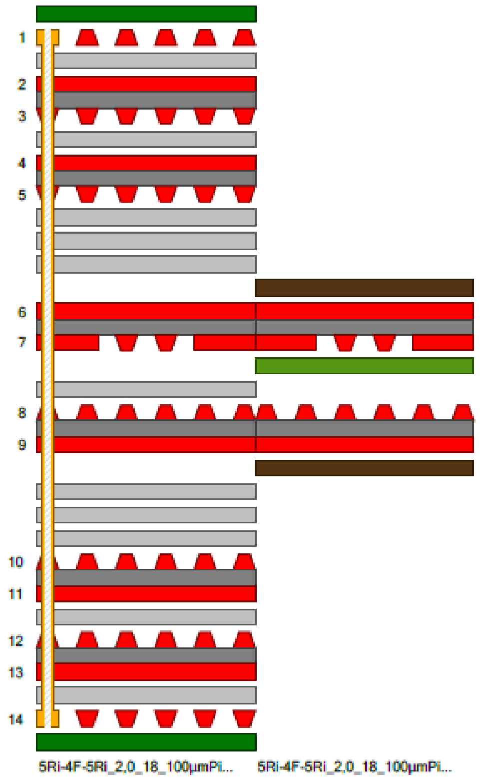
Calculation and Documentation 5Ri-4F-5Ri



Layer	Stack up	Description	Type	εr	Processed Thickness	Mask Thickness	Impedance ID
	450 +10,00% / -10,00%	LF-0110	Coverlay	3,60	50,00		
6					18,00		
		AP-8545R	Polyimide	3,40	100,00		
7					18,00		1, 2, 3, 4
		LF-0121	Bondply	3,60	100,00		
8					18,00		5, 6
		AP-8545R	Polyimide	3,40	100,00		
9					18,00		
		LF-0110	Coverlay	3,60	50,00		

Copper Thickness = 72,000 | Dielectric Thickness = 400,000 | Solder Mask Thickness = 0,000 | Stack Up Thickness = 472,000 | Stack Up Thickness with Soldermask = 472,000 |

Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Target Impedance	Calculated Impedance	Tol (+/- %)	Lower Trace Width (W1)	Trace Separation (S1)
1		Offset Stripline 1B2A	7	6	9	50,00	49,74	10,00	125,00	0,00
2		Edge Coupled Offset Stripline 1B2A	7	6	9	100,00	100,78	10,00	100,00	150,00
3		Offset Stripline 1B2A	7	6	9	40,00	39,79	10,00	190,00	0,00
4		Edge Coupled Offset Stripline 1B2A	7	6	9	80,00	80,02	10,00	165,00	150,00
5		Offset Stripline 1B1A	8	7	9	40,00	40,42	10,00	125,00	0,00
6		Edge Coupled Offset Stripline 1B1A	8	7	9	80,00	79,70	10,00	120,00	150,00

Notes

StackName: 5Ri-4F-5Ri_2,0_18_100µmPi/FLEX	Version:	Revision:	Modification:	Date of Revision:	Editor	Page 5/5	WÜRTH ELEKTRONIK
Date: 06.08.14	Associated Documents:						
Author: W.Öchslen							
Department:							
Site:							

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Agenda

- Interfaces
- Signal integrity with Flex-rigid
- Design Chain – Concept Flow
- Applications
- Summary, Q&A

Application
Starting Situation

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Power Board
8 layers
FR4

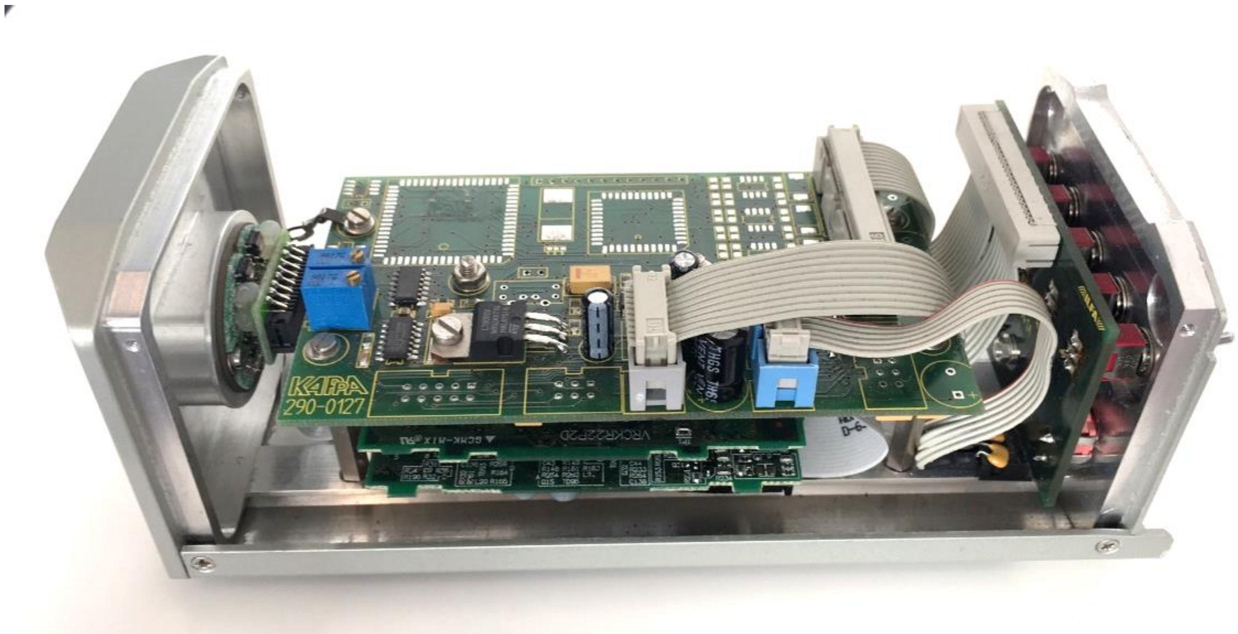
Connector Board
10 layers
FR4
contr. Impedance

€

FPGA Board
16 layers
high Tg FR4
contr. Impedance

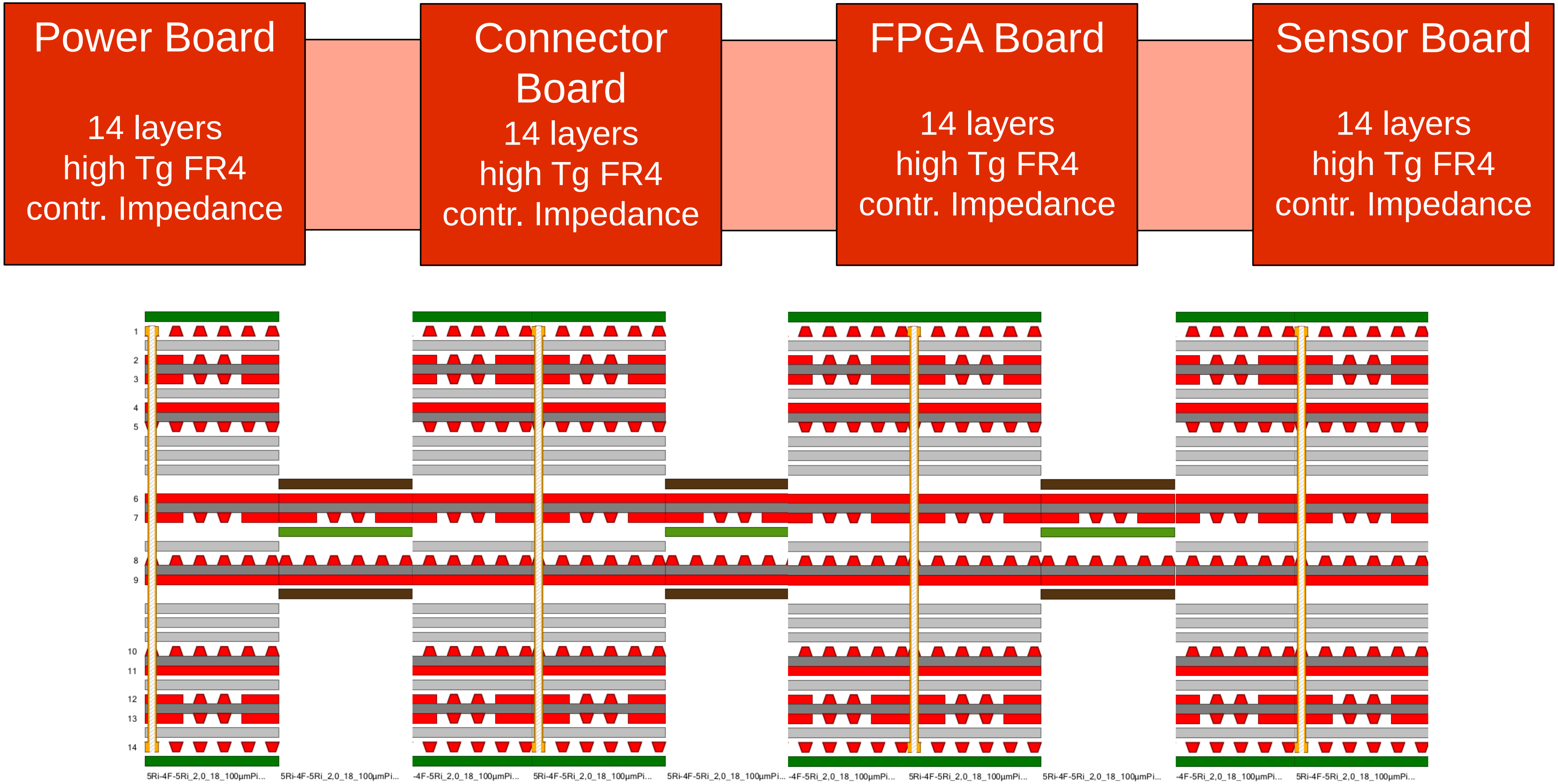
€

Sensor Board
10 layers
FR4
contr. Impedance



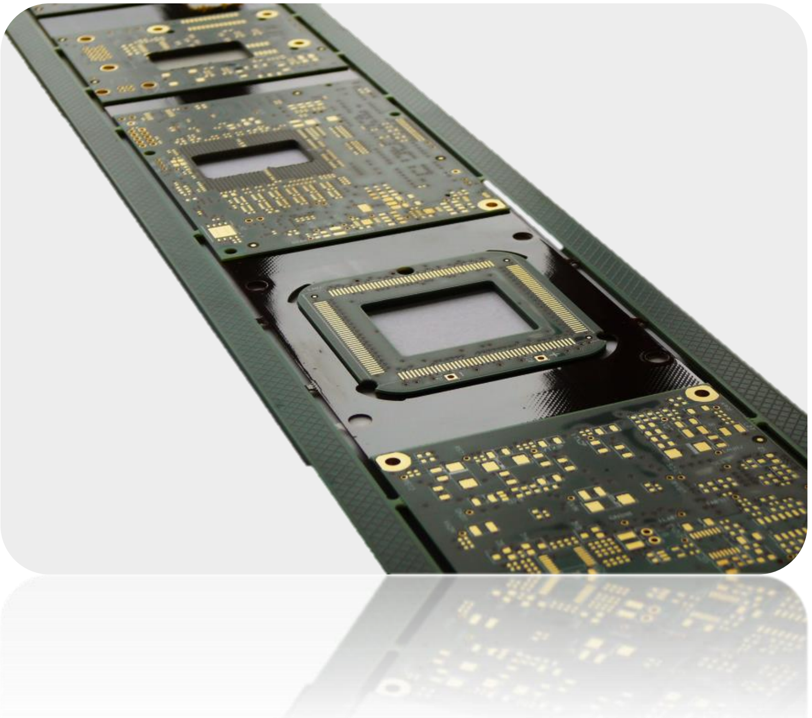
picture as example

Application
Approach: Flex-rigid xRi-4F-xRi



Application
Solution: Flex-rigid 4Ri-4F-4Ri

Power Board	Connector Board	FPGA Board	Sensor Board
12 layers high Tg FR4 contr. Impedance	12 layers high Tg FR4 contr. Impedance	12 layers high Tg FR4 contr. Impedance	12 layers high Tg FR4 contr. Impedance



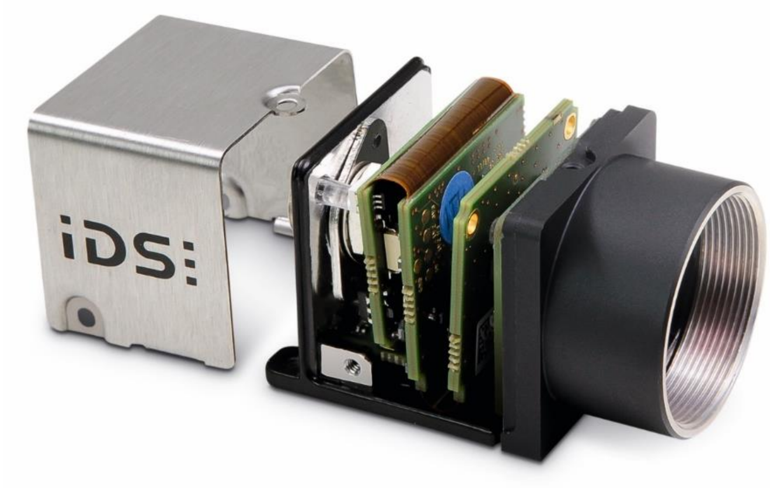
source: ANDOR

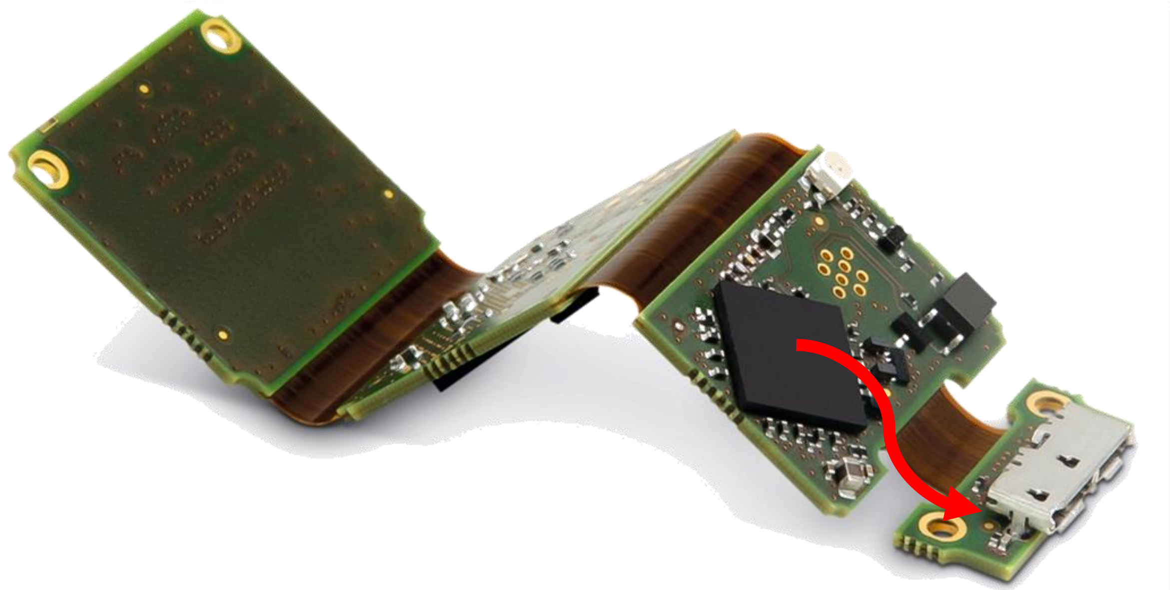
Miniaturization, Performance, Testability

WÜRTH ELEKTRONIK

USB3 Camera – Miniaturization at it´s best!

- USB connector on seperate rigid part
- impedance matched connected with flex part
- Avoiding connectors, saving Footprint areas
- Design uses Microvias
- excellent Performance
- good Testability
- good Robustness





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Agenda

- Interfaces
- Signal integrity with Flex-rigid
- Design Chain – Concept Flow
- Applications
- Summary, Q&A

Summary

<u>Flex-rigid for high data rates i.e. USB3</u>

- **high data rates require improved pcb solutions**
- **Flex-rigid technology shows intrinsic advantages**
- **the complexity of electronic design and development requires a close co-operation with the pcb producer**
- **Würth Elektronik has a lot of experience in producing impedance controlled flex-rigid pcbs**
- **for the implementation of USB3.1 Gen.2 in miniaturized Systems Flex-rigid technology seems to be an enabling technology**

Thank you very much for your time and your attention!

more than you expect

Andreas Schilpp
WÜRTH ELEKTRONIK GmbH & Co. KG
Senior Product Manager

Circuit Board Technology
T.: +49 7940 946 330

E. andreas.schilpp@we-online.de
W. www.we-online.de/flex